

Simulation Methods For ESD Protection Development By Harald Gossner

Simulation Methods for ESD Protection Development System Level ESD Protection Electrostatic Discharge Protection and Latch-Up Design and Methodologies for ASIC Development Advances in Solid State Circuit Technologies ESD in Silicon Integrated Circuits Analog Circuit Design Low-Power Electronics Design IBM Journal of Research and Development Electrostatic Discharge Protection Nanometer CMOS ICs Low-Power CMOS Circuits Electrical Overstress/Electrostatic Discharge Symposium Proceedings ESD Design, Characterization and Analysis of Electrostatic Discharge (ESD) Protection Solutions in Emerging and Modern Technologies Proceedings On-Chip Electro-Static Discharge (ESD) Protection for Radio-Frequency Integrated Circuits IEEE 1985 International Symposium on Electromagnetic Compatibility Science & Technology in Japan ESD in Silicon Integrated Circuits Electronic Design Harald Gossner Vladislav Vashchenko Steven H. Voldman Paul Chu E. Ajith Amerasekera Arthur H.M. van Roermund Christian Piguet Juin J. Liou Harry J.M. Veendrick Christian Piguet Steven H. Voldman Wen Liu Qiang Cui E. Ajith Amerasekera

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simulation methods for esd protection development looks at the integration of new techniques into a comprehensive development flow which is now available due advances made in the field during the recent years these findings allow for an early stable esd concept at a very early stage of the technology development which is essential now development cycles have been reduced the book also offers ways of increasing the optimization and control of the

technology concerning performance thus making the process more cost effective and increasingly efficient this title provides a guide through the latest research and technology presenting the esd protection development methodology this is based on a combination of process device and circuit stimulation and addresses the optimization of the industry critical issue reduced development cycles written to address the needs of the esd engineer this text is required reading by all industry practitioners and researchers and students within this field the first extensive overview on the subject of esd simulation addresses the industry critical issue of reduced development cycles and provides solutions presents the latest research in the field with high practical relevance and its results

this book addresses key aspects of analog integrated circuits and systems design related to system level electrostatic discharge esd protection it is an invaluable reference for anyone developing systems on chip soc and systems on package sop integrated with system level esd protection the book focuses on both the design of semiconductor integrated circuit ic components with embedded on chip system level protection and ic system co design the readers will be enabled to bring the system level esd protection solutions to the level of integrated circuits thereby reducing or completely eliminating the need for additional discrete components on the printed circuit board pcb and meeting system level esd requirements the authors take a systematic approach based on ic system esd protection co design a detailed description of the available ic level esd testing methods is provided together with a discussion of the correlation between ic level and system level esd testing methods the ic level esd protection design is demonstrated with representative case studies which are analyzed with various numerical simulations and esd testing the overall methodology for ic system esd co design is presented as a step by step procedure that involves both esd testing and numerical simulations

electrostatic discharge esd has been an issue in devices circuits and systems for electronics for many decades as early as the 1970s and continued to be an issue until today in this chapter the issue of esd protection design and methods for application specific integrated circuits asics will be discussed the chapter will discuss esd design in an asic environment the discussion will address esd design layout design rules and practices and the method of integration of esd protection into the asic design practice part of the methodology is the floor planning of an asic design i o library integration of esd into i o cells power distribution and placement of power pads in both array and peripheral design methodologies as part of the asic i o design guard rings and latch up interactions will be highlighted

this book brings together contributions from experts in the fields to describe the current status of important topics in solid state circuit technologies it consists of 20 chapters which are grouped under the following categories general information circuits and devices materials and characterization

techniques these chapters have been written by renowned experts in the respective fields making this book valuable to the integrated circuits and materials science communities it is intended for a diverse readership including electrical engineers and material scientists in the industry and academic institutions readers will be able to familiarize themselves with the latest technologies in the various fields

examines the various methods available for circuit protection including coverage of the newly developed esd circuit protection schemes for vlsi circuits provides guidance on the implementation of circuit protection measures includes new sections on esd design rules layout approaches package effects and circuit concepts reviews the new charged device model cdm test method and evaluates design requirements necessary for circuit protection

number 12 in the successful series of analog circuit design provides valuable information and excellent overviews of analogue circuit design cad and rf systems the series is an ideal reference for those involved in analogue and mixed signal design

the power consumption of integrated circuits is one of the most problematic considerations affecting the design of high performance chips and portable devices the study of power saving design methodologies now must also include subjects such as systems on chips embedded software and the future of microelectronics low power electronics design covers all major aspects of low power design of ics in deep submicron technologies and addresses emerging topics related to future design this volume explores in individual chapters written by expert authors the many low power techniques born during the past decade it also discusses the many different domains and disciplines that impact power consumption including processors complex circuits software cad tools and energy sources and management the authors delve into what many specialists predict about the future by presenting techniques that are promising but are not yet reality they investigate nanotechnologies optical circuits ad hoc networks e textiles as well as human powered sources of energy low power electronics design delivers a complete picture of today s methods for reducing power and also illustrates the advances in chip design that may be commonplace 10 or 15 years from now

electrostatic discharge esd is one of the most prevalent threats to electronic components in an esd event a finite amount of charge is transferred from one object i e human body to another i e microchip this process can result in a very high current passing through the microchip within a very short period of time thus more than 35 percent of single event chip damages can be attributed to esd events and designing esd structures to protect integrated circuits against the esd stresses is a high priority in the semiconductor industry electrostatic discharge protection advances and applications delivers timely coverage of component and system level esd protection for semiconductor devices and integrated circuits bringing together contributions from

internationally respected researchers and engineers with expertise in ESD design optimization modeling simulation and characterization this book bridges the gap between theory and practice to offer valuable insight into the state of the art of ESD protection amply illustrated with tables figures and case studies the text instills a deeper understanding of ESD events and ESD protection design principles examines vital processes including Si CMOS Si BCD Si SOI and GaN technologies addresses important aspects pertinent to the modeling and simulation of ESD protection solutions electrostatic discharge protection advances and applications provides a single source for cutting edge information vital to the research and development of effective robust ESD protection solutions for semiconductor devices and integrated circuits

this textbook provides a comprehensive fully updated introduction to the essentials of nanometer CMOS integrated circuits it includes aspects of scaling to even beyond 12nm CMOS technologies and designs it clearly describes the fundamental CMOS operating principles and presents substantial insight into the various aspects of design implementation and application coverage includes all associated disciplines of nanometer CMOS ICs including physics lithography technology design memories VLSI power consumption variability reliability and signal integrity testing yield failure analysis packaging scaling trends and road blocks the text is based upon in house Philips NXP semiconductors applied materials ASML imec ST Ericsson TSMC etc courseware which to date has been completed by more than 4500 engineers working in a large variety of related disciplines architecture design test fabrication process packaging failure analysis and software

the power consumption of microprocessors is one of the most important challenges of high performance chips and portable devices in chapters drawn from Piguet's recently published low power electronics design low power CMOS circuits technology logic design and CAD tools addresses the design of low power circuitry in deep submicron technologies it provides a focused reference for specialists involved in designing low power circuitry from transistors to logic gates the book is organized into three broad sections for convenient access the first examines the history of low power electronics along with a look at emerging and possible future technologies it also considers other technologies such as nanotechnologies and optical chips that may be useful in designing integrated circuits the second part explains the techniques used to reduce power consumption at low levels these include clock gating leakage reduction interconnecting and communication on chips and adiabatic circuits the final section discusses various CAD tools for designing low power circuits this section includes three chapters that demonstrate the tools and low power design issues at three major companies that produce logic synthesizers providing detailed examinations contributed by leading experts low power CMOS circuits technology logic design and CAD tools supplies authoritative information on how to design and model for high performance with low power consumption in modern integrated circuits it is a must read for anyone designing modern computers or embedded systems

with the growth of high speed telecommunications and wireless technology it is becoming increasingly important for engineers to understand radio frequency rf applications and their sensitivity to electrostatic discharge esd phenomena this enables the development of esd design methods for rf technology leading to increased protection against electrical overstress eos and esd esd rf technology and circuits presents methods for co synthesizing esd networks for rf applications to achieve improved performance and esd protection of semiconductor chips discusses rf esd design methods of capacitance load transformation matching network co synthesis capacitance shunts inductive shunts impedance isolation load cancellation methods distributed loads emitter degeneration buffering and ballasting examines esd protection and design of active and passive elements in rf complementary metal oxide semiconductor cmos rf laterally diffused metal oxide semiconductor ldmos rf bicmos silicon germanium sige rf bicmos silicon germanium carbon sige and gallium arsenide technology gives information on rf esd testing methodologies rf degradation effects and failure mechanisms for devices circuits and systems highlights rf esd mixed signal design integration of digital analog and rf circuitry sets out examples of rf esd design computer aided design methodologies covers state of the art rf esd input circuits as well as voltage triggered to rc triggered esd power clamps networks in rf technologies as well as off chip protection concepts following the authors series of books on esd this book will be a thorough overview of esd in rf technology for rf semiconductor chip and esd engineers device and circuit engineers working in the rf domain and quality reliability and failure analysis engineers will also find it a valuable reference in the rapidly growing area of rf esd design in addition it will appeal to graduate students in rf microwave technology and rf circuit design

electrostatic discharge esd is a significant hazard to electronic components and systems based on a specific processing technology a given circuit application requires a customized esd consideration that includes the devices operating voltage leakage current breakdown constraints and footprint as new technology nodes mature every 3 5 years design of effective esd protection solutions has become more and more challenging due to the narrowed design window elevated electric field and current density as well as new failure mechanisms that are not well understood the endeavor of this research is to develop novel effective and robust esd protection solutions for both emerging technologies and modern complementary metal oxide semiconductor cmos technologies the si nanowire field effect transistors are projected by the international technology roadmap for semiconductors as promising next generation cmos devices due to their superior dc and rf performances as well as ease of fabrication in existing silicon processing aiming at proposing esd protection solutions for nanowire based circuits the dimension parameters fabrication process and layout dependency of such devices under human body mode hbm esd stresses are studied experimentally in company with failure analysis revealing the failure mechanism induced by esd the findings including design methodologies failure mechanism and technology comparisons should provide practical knowhow of the development of esd protection schemes

for the nanowire based integrated circuits organic thin film transistors OTFTs are the basic elements for the emerging flexible printable large area and low cost organic electronic circuits although there are plentiful studies focusing on the DC stress induced reliability degradation the operation mechanism of OTFTs subject to ESD is not yet available in the literature and are urgently needed before the organic technology can be pushed into consumer market in this work the ESD operation mechanism of OTFT depending on gate biasing condition and dimension parameters are investigated by extensive characterization and thorough evaluation the device degradation evolution and failure mechanism under ESD are also investigated by specially designed experiments in addition to the exploration of ESD protection solutions in emerging technologies efforts have also been placed in the design and analysis of a major ESD protection device diode triggered silicon controlled rectifier DTSCR in modern CMOS technology 90nm bulk on the one hand a new type DTSCR having bi directional conduction capability optimized design window high HBM robustness and low parasitic capacitance are developed utilizing the combination of a bi directional silicon controlled rectifier and bi directional diode strings on the other hand the HBM and charged device mode CDM ESD robustness of DTSCRs using four typical layout topologies are compared and analyzed in terms of trigger voltage holding voltage failure current density turn on time and overshoot voltage the advantages and drawbacks of each layout are summarized and those offering the best overall performance are suggested at the end

this book enables readers to design effective ESD protection solutions for all mainstream RF fabrication processes GaAs PHEMT SiGe HBT CMOS the new techniques introduced by the authors have much higher protection levels and much lower parasitic effects than those of existing ESD protection devices the authors describe in detail the ESD phenomenon as well as ESD protection fundamentals standards test equipment and basic design strategies readers will benefit from realistic case studies of ESD protection for RFICs and will learn to increase significantly modern RFICs ESD safety level while maximizing RF performance

ESD in silicon integrated circuits Ajith Amerasekera Charvaka Duvvury Texas Instruments Inc Dallas USA electrostatic discharge ESD effects in silicon integrated circuits have become a major concern as today's high circuit density technologies shrink to sub micro dimensions this book provides an understanding of the basic features related to ESD and deals with topics ranging from the physics of devices operating under ESD conditions to approaches for solving and improving ESD performance in advanced ICs features include description of the methods used to reproduce ESD type events in a controlled test environment analysis of the behavior of different semiconductor devices under ESD conditions including the physics and modeling of devices detailed study of design and layout requirements for ESD protection circuits case studies showing examples of approaches to solving ESD design problems including failure analysis covering the state of the art in circuit design for ESD prevention this practical book is written from an industrial perspective and will appeal to engineers and scientists working in the fields of IC and transistor design researchers and advanced students in the fields of device circuit modeling and

semiconductor reliability seeking to understand the fundamentals of ESD phenomena will also find this book an invaluable reference source

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